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EXAMINER

SPITTLE, MATTHEW D

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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/644,133	Applicant(s) KARAMATAS ET AL.	
	Examiner Matthew D. Spittle	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11/2/2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10, 12-19 and 21-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 12-19 and 21-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 1 – 10, 12 – 19, and 21 – 30 have been examined.

Claim Rejections - 35 USC § 101

5 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10 Claims 16 and 21 are directed to non-statutory intangible embodiments. In view of Applicant's disclosure, paragraph 16 the medium is not limited to tangible embodiments, instead being defined as both tangible embodiments (e.g., [ROM, RAM, magnetic disk storage media, optical storage media, flash memory]) and
15 intangible embodiments (e.g., [electrical, optical, acoustic, carrier waves, infrared signals, digital signals]). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

For claim 16, Examiner recommends revising it to read (in part):

"An article of manufacture comprising:

a computer-readable storage medium; and,

20 means in the medium, executed by a processor, for assigning interrupts..."

or

"...a computer-readable storage medium; and,

means in the medium for assigning, under processor control, interrupts..."

- 25 For claim 21, Examiner recommends revising it to read (in part):
- “A computer-readable storage medium comprising:...”
- or
- “An article of manufacture comprising:
- a processor; and
- 30 an interrupt-assignor executed by the processor to assign interrupts...”

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

- 35 The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
- 40 Claims 1 – 10, 12 – 19, and 21 – 30 are rejected under 35 U.S.C. 112, first
- paragraph, as failing to comply with the enablement requirement. The claim(s) contains
- subject matter which was not described in the specification in such a way as to enable
- one skilled in the art to which it pertains, or with which it is most nearly connected, to
- make and/or use the invention. Claims 1 – 10, 12 – 19, and 21 – 30 recite one or more
- 45 of the nodes being processorless **and** memoryless. Applicant's disclosure in paragraph
- 22 describes that other nodes may not include either processors **or** memory. For the
- purpose of applying prior art, Examiner will assume the claim reads “...”processorless
- or** memoryless.”

50 The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

 Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite
55 for failing to particularly point out and distinctly claim the subject matter which applicant
 regards as the invention.

 Claim 7 recites "...each of one or more of the nodes..." in lines 7 and 8.

Examiner recommends deleting the phrase "each of" in both instances.

60

Claim Rejections - 35 USC § 103

 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all
obviousness rejections set forth in this Office action:

65 (a) A patent may not be obtained though the invention is not identically disclosed or described as set
 forth in section 102 of this title, if the differences between the subject matter sought to be patented and
 the prior art are such that the subject matter as a whole would have been obvious at the time the
 invention was made to a person having ordinary skill in the art to which said subject matter pertains.
 Patentability shall not be negated by the manner in which the invention was made.

70

 The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148
USPQ 459 (1966), that are applied for establishing a background for determining
obviousness under 35 U.S.C. 103(a) are summarized as follows:

- 75 1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating
 obviousness or nonobviousness.

80 Claims 1 – 10, 12 – 19, and 21 – 30 are rejected under 35 U.S.C. 103(a) as
being unpatentable over Kiick (U.S. Pub. 2003/0200250) in view of Carpenter et al.
(U.S. 6,148,361).

 Regarding claim 1, Kiick teaches a method comprising at least one of:

 Assigning interrupts for a plurality of input/output (I/O) devices among a plurality
85 of nodes of a system based on at least one of: the nodes to which the I/O devices are
connected; the nodes at which interrupt service routines for the I/O devices reside; and
processors of the nodes for the nodes having processors, where one or more of the
nodes have processors and memory (Paragraph 34 describes that interrupts should be
assigned to the “closest” processors, and not across node boundaries. Examiner
90 interprets this to mean the interrupts for the I/O devices should be assigned to nodes to
which they are connected or to nodes where the ISRs for the said I/O devices reside.);

 For each node of the system having processors, assigning the interrupts for the
devices that are performance critical and that have been assigned to the node among
the processors of the node in a round-robin manner (Examiner interprets all devices in
95 the reference to be considered “performance critical”; Paragraph 26);

 Dynamically modifying assignments of the interrupts among the nodes of the
system based on actual performance characteristics of the assignments (Paragraphs
25, 28, 31);

 For each node of the system having processors, dynamically modifying
100 assignments of the interrupts that are performance critical and that have been assigned

to the node among the processors of the node based on actual performance characteristics of the assignments (Paragraphs 25, 28, 31).

Kiick fails to teach where one or more of the nodes are processorless or memoryless.

105 Carpenter et al. teach that it may be advantageous to expand system memory without increasing the processing resources of a NUMA system by adding a processorless node (column 12, lines 15 – 20).

 Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate a processorless node as taught by
110 Carpenter et al. into the system of Kiick for the purpose of increasing the system memory without increasing the processing resources. This would have been obvious in order to improve the storage capability of the system without also incurring the additional (and unnecessary) cost of an additional processor.

115 With regard to claim 2, Kiick teaches the method of claim 1, wherein assigning the interrupts for the plurality of I/O device among the plurality of nodes of the system comprises, for each I/O device:

 Where the node (Figure 1, items 102A, 102B) to which the I/O device (Figure 1, items 110A, 110B) is connected has a cache (Paragraph 10), memory (Figure 1, items
120 108A, 108B), and at least one processor (Figure 1, items 106A, 106B), assigning the interrupt for the I/O device to the node to which the I/O device is connected;

Otherwise, where the node at which the interrupt service routine for the I/O device resides has memory and at least one processor, assigning the interrupt for the I/O device to the node at which the interrupt service routine for the I/O device resides
125 (Paragraph 34 describes that interrupts should be assigned to the “closest” processors, and not across node boundaries. Examiner interprets this to mean the interrupts for the I/O devices should be assigned to nodes to which they are connected or to nodes where the ISRs for the said I/O devices reside.).

130 With regard to claim 3, Kiick describes the method of claim 2, wherein assigning the interrupts for the plurality of I/O devices among the plurality of nodes of the system further comprises, for each I/O device, otherwise, assigning the interrupt for the I/O device to one of the nodes having memory and at least one processor (Paragraph 23 describes each node containing memory (Figure 1, items 108A, 108B), and at least one
135 processor (Figure 1, items 106A, 106B); paragraph 26).

With regard to claim 4, Kiick teaches the method of claim 1, wherein dynamically modifying the assignments of the interrupts among the nodes of the system comprises:

Measuring responsiveness of the node in processing the interrupt (paragraphs
140 27 – 30);

Kiick fails to explicitly teach assigning the interrupt to the node at which the interrupt service routine for the I/O device resides; measuring responsiveness of the node at which the interrupt service routine for the I/O device resides in processing the

interrupt; and where the responsiveness of the node to which the I/O device is
145 connected is better than the responsiveness of the node at which the interrupt service
routine for the I/O device resides, reassigning the interrupt to the node to which the I/O
device is connected.

Kiick does, however, teach that the dynamic interrupt distributor should be aware
of the system architecture, and re-assign interrupts to the “closest” processors
150 (paragraph 34). Therefore, it would have been obvious to one of ordinary skill in this art
at the time of invention by Applicant to give preference in assigning interrupts to nodes
at which the ISR for the device resides, or at which the I/O device itself resides, and
then to re-assign interrupts accordingly to which configuration produced better
performance as described in paragraphs 28 – 30).

155
With regard to claim 5, Kiick teaches the method of claim 4, wherein dynamically
modifying the assignments of the interrupts among the nodes of the system comprises,
for each assignment of an interrupt for an I/O device to a node, where the node is that
at which the interrupt service routine for the I/O device resides:

160 Measuring responsiveness of the node in processing the interrupt (paragraphs
27 – 30);

Kiick fails to explicitly teach assigning the interrupt to the node to which the I/O
device is connected; measuring responsiveness of the node to which the I/O device is
connected in processing the interrupt; and where the responsiveness of the node at
165 which the interrupt service routine for the I/O device is connected is better than the

responsiveness of the node to which the I/O device is connected, reassigning the interrupt to the node at which the interrupt service routine for the I/O device resides.

Kiick does, however, teach that the dynamic interrupt distributor should be aware of the system architecture, and re-assign interrupts to the "closest" processors

170 (paragraph 34). Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to give preference in assigning interrupts to nodes at which the I/O device is connected, or at which the ISR for the I/O device itself resides, and then to re-assign interrupts accordingly to which configuration produced better performance as described in paragraphs 28 – 30).

175

With regard to claim 6, Kiick teaches the method of claim 1, wherein for each node of the system, dynamically modifying the assignments of the interrupts that are performance critical and that have been assigned to the node among the processors of the node comprises:

180 Measuring the responsiveness of the processors of the node in processing the interrupts assigned thereto (paragraphs 27, 28, 35);

Where a differential between a best responsiveness and a worst responsiveness is greater than a threshold (paragraph 28; where a threshold may be interpreted as a "large enough difference");

185 Reassigning at least one of the interrupts assigned to the processor having the worst responsiveness to the processor having the best responsiveness (paragraphs 27 – 30, 35).

With regard to claim 7, Kiick teaches a non-uniform memory access (NUMA)

190 system comprising:

A plurality of nodes (Figure 1, items 102A, 102B);

A plurality of input/output (I/O) devices, each I/O device connected to one of the plurality of nodes and having an interrupt (Figure 1, items 110A, 110B);

195 An interrupt-assignor responsive to the I/O devices and the nodes to assign the interrupt for each I/O device to one of the plurality of nodes in a performance-optimized manner (where an interrupt-assignor may be interpreted as a dynamic interrupt distributor; Figure 2, item 210; paragraphs 25, 28).

200 Kiick teaches a multiprocessor system that is tightly-coupled, and could have shared main memory, mass storage, and cache, and runs a single copy of an operating system (paragraph 7). These limitations define a NUMA system as evidenced by the definition from www.whatis.com, and therefore, Kiick implicitly describes a NUMA system for use with his invention.

Kiick fails to teach where one or more of the nodes are processorless or memoryless.

205 Carpenter et al. teach that it may be advantageous to expand system memory without increasing the processing resources of a NUMA system by adding a processorless node (column 12, lines 15 – 20).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate a processorless node as taught by

210 Carpenter et al. into the system of Kiick for the purpose of increasing the system memory without increasing the processing resources. This would have been obvious in order to improve the storage capability of the system without also incurring the additional (and unnecessary) cost of an additional processor.

215 With regard to claim 8, Kiick teaches the system of claim 7, wherein the memory of each node that has memory is local to the node and remote to all other nodes (Figure 1, items 108A, 108B; paragraph 23 describes each domain having domain-specific memory (where a domain may be interpreted as a node, as described earlier in paragraph 23)), and the interrupt-assignor is to assign the interrupt for each I/O device
220 to one of the plurality of nodes that has memory and at least one processor (where an interrupt-assignor may be interpreted as a dynamic interrupt distributor; Figure 2, item 210; paragraphs 25, 28; all nodes (items 102A, 102B are shown in Figure 1 to have memory and at least one processor).

225 With regard to claim 9, Kiick teaches the system of claim 8, wherein at least one of the I/O devices are performance critical, the interrupt-assignor further to assign the interrupt for each I/O device that is performance critical among the at least one processor of the node to which the interrupt has been assigned in a round-robin manner (Examiner interprets all of the I/O devices of the invention of Kiick to be performance
230 critical, thereby necessitating the use of his invention to improve performance; Paragraphs 25, 26, 28).

235 With regard to claim 10, Kiick describes the system of claim 7, wherein, for each node that has processors, the interrupt-assignment software is further to dynamically modify assignments of the interrupts that are performance critical among the at least one processor of the node based on actual performance characteristics of the assignments. Examiner believes Applicant meant to refer to "the interrupt-assignor" instead of "interrupt-assignment software." (Paragraphs 26, 28, 31).

240 With regard to claim 12, Kiick describes the system of claim 7, wherein the interrupt-assignor is further to dynamically modify assignments of the interrupts among the plurality of nodes based on actual performance characteristics of the assignments (Paragraphs 26, 28, 31).

245 Regarding claim 13, Kiick teaches wherein the interrupt-assignor (paragraph 34, where a interrupt-assignor may be interpreted as a dynamic interrupt distributor) is to give primary preference in assigning the interrupt for each I/O device to the node to which the I/O device is connected (paragraph 34, where a domain may be interpreted as a node) where the node to which the I/O device is connected has a cache
250 (paragraph 10; Examiner interprets the processors within the processor complex (106A, 106B) as having on-chip cache), memory (Figure 1, items 108A, 108B) , and at least one processor (Figure 1, items 106A, 106B).

Regarding claim 14, Kiick teaches wherein each I/O device further has an
255 interrupt service routine residing at one of the plurality of nodes, and the interrupt-
assignor (paragraph 34, where a interrupt-assignor may be interpreted as a dynamic
interrupt distributor) is to give secondary preference in assigning the interrupt for each
I/O device to the node at which the interrupt service routine of the I/O device resides
(paragraphs 28, 34; Examiner notes that paragraph 28 identifies re-assigning interrupts
260 to be equivalent to re-assigning ISRs) where the node at which the interrupt service
routine of the I/O device resides has a cache (paragraph 10; Examiner interprets the
processors within the processor complex (106A, 106B) as having on-chip cache),
memory (Figure 1, items 108A, 108B), and at least one processor ((Figure 1, items
106A, 106B).

265

With regard to claim 15, Kiick describes the system of claim 7, wherein the
interrupt-assignor resides within one of the plurality of nodes (where an interrupt-
assignor may be interpreted as a dynamic interrupt distributor; Figure 2, item 210;
paragraph 28 describes a predetermined processor in a domain (node) dedicated to run
270 the interrupt-assignor).

With regard to claim 16, Kiick teaches an article of manufacture comprising:

A computer readable medium;

Means in the medium for assigning interrupts for a plurality of input/output (I/O)
275 devices (paragraph 28 describes a dynamic interrupt distributor embodied as a program

module. Examiner identifies that a program module must be embodied on a computer readable medium in order to be useful, and therefore implicitly describes this limitation) among a plurality of nodes based on at least one factor selected from the set consisting of: the nodes to which the devices are connected, and the nodes at which interrupt
280 service routines for the I/O devices reside (Paragraph 34 describes that interrupts should be assigned to the "closest" processors, and not across node boundaries. Examiner interprets this to mean the interrupts for the I/O devices should be assigned to nodes to which they are connected or to nodes where the ISRs for the said I/O devices reside.), where one or more of the nodes have processors and memory.

285 Kiick fails to teach where one or more of the nodes are processorless or memoryless.

Carpenter et al. teach that it may be advantageous to expand system memory without increasing the processing resources of a NUMA system by adding a processorless node (column 12, lines 15 – 20).

290 Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate a processorless node as taught by Carpenter et al. into the system of Kiick for the purpose of increasing the system memory without increasing the processing resources. This would have been obvious in order to improve the storage capability of the system without also incurring the
295 additional (and unnecessary) cost of an additional processor.

With regard to claim 17, Kiick teaches the article of claim 16, wherein the means is for assigning the interrupts among the plurality of nodes further based on whether the nodes have processors and memories (Kiick describes assigning ISRs to processors
300 which have associated memories; paragraph 14).

With regard to claim 18, Kiick describes the article of claim 16, wherein the means, for each node having processors, is further for assigning the interrupts for the devices that are performance critical and that have been assigned to the node among
305 the processors of the node in a round-robin manner (Examiner interprets all of the I/O devices of the invention of Kiick to be performance critical, thereby necessitating the use of his invention to improve performance; Paragraphs 25, 26, 28).

With regard to claim 19, Kiick describes the article of claim 18, wherein the
310 means, is further for dynamically modifying assignments of the interrupts among the nodes based on actual performance characteristics of the assignments, and, for each node having processors, for dynamically modifying assignments of the interrupts that are performance critical and that have been assigned to the node among the processors of the node based on actual performance characteristics of the assignments
315 (paragraphs 25, 28, 31).

With regard to claim 21, teaches describes an article of manufacture comprising:

An interrupt-assignor (Figure 2, item 210; paragraph 28) to assign interrupts for a plurality of input/output (I/O) devices among a plurality of nodes based on at least one
320 factor selected from the set consisting of:

The nodes to which the I/O devices are connected;

The nodes at which interrupt service routines for the I/O devices reside, where one or more of the nodes have processors and memory.

(Paragraph 34 describes that interrupts should be assigned to the "closest"
325 processors, and not across node boundaries. Examiner interprets this to mean the interrupts for the I/O devices should be assigned to nodes to which they are connected or to nodes where the ISRs for the said I/O devices reside.).

Kiick fails to teach where one or more of the nodes are processorless or memoryless.

330 Carpenter et al. teach that it may be advantageous to expand system memory without increasing the processing resources of a NUMA system by adding a processorless node (column 12, lines 15 – 20).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate a processorless node as taught by
335 Carpenter et al. into the system of Kiick for the purpose of increasing the system memory without increasing the processing resources. This would have been obvious in order to improve the storage capability of the system without also incurring the additional (and unnecessary) cost of an additional processor.

340 With regard to claim 22, Kiick teaches the article of claim 216, wherein the means is for assigning the interrupts among the plurality of nodes further based on whether the nodes have processors and memories (Kiick describes assigning ISRs to processors which have associated memories; paragraph 14).

345 With regard to claim 23, Kiick teaches the article of claim 21, wherein the interrupt-assignor is to assign, for each node, the interrupts for the devices that are performance critical and that have been assigned to the node among the processors of the node in a round-robin manner (where the interrupt-assignor may be interpreted as a dynamic interrupt distributor; Examiner interprets all of the I/O devices of the invention
350 of Kiick to be performance critical, thereby necessitating the use of his invention to improve performance; Paragraphs 25, 26, 28).

 With regard to claim 24, Kiick teaches the article of claim 23, wherein the interrupt-assignor is to dynamically modify assignments of the interrupts among the
355 nodes based on actual performance characteristics of the assignments, and, for each node having processors, to dynamically modify assignments of the interrupts that are performance critical and that have been assigned to the node among the processors of the node based on actual performance characteristics of the assignments (where an interrupt-assignor may be interpreted as a dynamic interrupt distributor; paragraphs 25,
360 28, 31).

With regard to claim 25, Kiick teaches a method comprising:

Assigning interrupts for a plurality of input/output (I/O) devices among a plurality of nodes based on at least one factor selected from the set consisting of: the nodes to
365 which the I/O devices are connected; and the nodes at which interrupt service routines for the I/O devices reside, where one or more of the nodes have processors and memory (Paragraph 34 describes that interrupts should be assigned to the "closest" processors, and not across node boundaries. Examiner interprets this to mean the interrupts for the I/O devices should be assigned to nodes to which they are connected
370 or to nodes where the ISRs for the said I/O devices reside.);

For each node of the system, assigning the interrupts for the devices that are performance critical and that have been assigned to the node among the processors of the node in a round-robin manner (Examiner interprets all of the I/O devices of the invention of Kiick to be performance critical, thereby necessitating the use of his
375 invention to improve performance; Paragraphs 25, 26, 28);

Dynamically modifying assignments of the interrupts among the nodes of the system based on actual performance characteristics of the assignments (paragraphs 25, 28, 31);

For each node of the system, dynamically modifying assignments of the
380 interrupts that are performance critical and that have been assigned to the node among the processors of the node based on actual performance characteristics of the assignments (paragraphs 25, 28, 31).

Kiick fails to teach where one or more of the nodes are processorless or memoryless.

385 Carpenter et al. teach that it may be advantageous to expand system memory without increasing the processing resources of a NUMA system by adding a processorless node (column 12, lines 15 – 20).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate a processorless node as taught by
390 Carpenter et al. into the system of Kiick for the purpose of increasing the system memory without increasing the processing resources. This would have been obvious in order to improve the storage capability of the system without also incurring the additional (and unnecessary) cost of an additional processor.

395 With regard to claim 26, Kiick teaches the method of claim 25, wherein assigning the interrupts for the plurality of I/O devices among the plurality of nodes of the system comprises, for each I/O device:

Where the node (Figure 1, items 102A, 102B) to which the I/O device (Figure 1, items 110A, 110B) is connected has a cache (Paragraph 10), memory (Figure 1, items
400 108A, 108B), and at least one processor (Figure 1, items 106A, 106B), assigning the interrupt for the I/O device to the node to which the I/O device is connected;

Otherwise, where the node at which the interrupt service routine for the I/O device resides has memory and at least one processor, assigning the interrupt for the I/O device to the node at which the interrupt service routine for the I/O device resides

405 (Paragraph 34 describes that interrupts should be assigned to the "closest" processors, and not across node boundaries. Examiner interprets this to mean the interrupts for the I/O devices should be assigned to nodes to which they are connected or to nodes where the ISRs for the said I/O devices reside.).

410 With regard to claim 27, Kiick teaches the method of claim 25, wherein assigning the interrupts for the plurality of I/O devices among the plurality of nodes of the NUMA system further comprises, for each I/O device, otherwise, assigning the interrupt for the I/O device to one of the nodes having memory and at least one processor (Paragraph 23 describes each node containing memory (Figure 1, items 108A, 108B), and at least
415 one processor (Figure 1, items 106A, 106B); paragraph 26).

With regard to claim 28, Kiick teaches the method of claim 25, wherein dynamically modifying the assignments of the interrupts among the nodes of the system comprises:

420 Measuring responsiveness of the node in processing the interrupt (paragraphs 27 – 30);

Kiick fails to explicitly teach assigning the interrupt to the node at which the interrupt service routine for the I/O device resides; measuring responsiveness of the node at which the interrupt service routine for the I/O device resides in processing the
425 interrupt; and where the responsiveness of the node to which the I/O device is connected is better than the responsiveness of the node at which the interrupt service

routine for the I/O device resides, reassigning the interrupt to the node to which the I/O device is connected.

430 Kiick does, however, teach that the dynamic interrupt distributor should be aware of the system architecture, and re-assign interrupts to the “closest” processors (paragraph 34). Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to give preference in assigning interrupts to nodes at which the ISR for the device resides, or at which the I/O device itself resides, and then to re-assign interrupts accordingly to which configuration produced better
435 performance as described in paragraphs 28 – 30).

With regard to claim 29, Kiick teaches the method of claim 25, wherein dynamically modifying the assignments of the interrupts among the nodes of the system comprises, for each assignment of an interrupt for an I/O device to a node, where the
440 node is that at which the interrupt service routine for the I/O device resides:

Measuring responsiveness of the node in processing the interrupt (paragraphs 27 – 30);

Kiick fails to explicitly teach assigning the interrupt to the node to which the I/O device is connected; measuring responsiveness of the node to which the I/O device is
445 connected in processing the interrupt; and where the responsiveness of the node at which the interrupt service routine for the I/O device is connected is better than the responsiveness of the node to which the I/O device is connected, reassigning the interrupt to the node at which the interrupt service routine for the I/O device resides.

Kiick does, however, teach that the dynamic interrupt distributor should be aware
450 of the system architecture, and re-assign interrupts to the “closest” processors
(paragraph 34). Therefore, it would have been obvious to one of ordinary skill in this art
at the time of invention by Applicant to give preference in assigning interrupts to nodes
at which the I/O device is connected, or at which the ISR for the I/O device itself resides,
and then to re-assign interrupts accordingly to which configuration produced better
455 performance as described in paragraphs 28 – 30).

With regard to claim 30, Kiick teaches the method of claim 25, wherein for each
node of the system having memory, dynamically modifying the assignments of the
interrupts that are performance critical and that have been assigned to the node among
460 the processors of the node comprises:

Measuring the responsiveness of the processors of the node in processing the
interrupts assigned thereto (paragraphs 27, 28, 35);

Where a differential between a best responsiveness and a worst responsiveness
is greater than a threshold (paragraph 28; where a threshold may be interpreted as a
465 “large enough difference”);

Reassigning at least one of the interrupts assigned to the processor having the
worst responsiveness to the processor having the best responsiveness (paragraphs 27
– 30, 35).

Applicant's arguments, filed 11/2/2006, with respect to the rejection(s) of claim(s) 1 - 30 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kiick in view of Carpenter et al.

475 Regarding Applicant's argument that Neal does not show memoryless and processorless nodes, Examiner agrees, and the rejection in view of Neal is withdrawn.

Conclusion

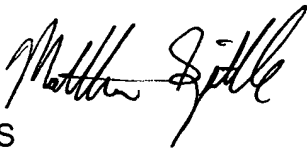
480 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

 If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for
485 the organization where this application or proceeding is assigned is 571-273-8300.

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